

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE AND TRADEMARK OFFICE

In re application of: ANNAPRAGADA et al.

Application No.: 09/688,021

Filed: October 13, 2000

Title: PROCESS FOR ETCHING VIAS IN ORGANOSILICATE GLASS MATERIALS

WITHOUT CAUSING RIE LAG

LAM1P154/P0696

Examiner: ANDERSON, Matthew

Group: 1765

CERTIFICATE OF MAILING

I hereby certify that this correspondence and the documents and/or fees referred to as attached therein are being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Box RCE, Commissioner for Patents, Washington, D.C. 20231, on February 19, 2003.

PRELIMINARY AMENDMENT C

Box RCE · Commissioner for Patents Washington, D.C. 20231

Dear Sir:

In response to the Office communication dated November 20, 2002 and the Advisory Action dated January 21, 2003, please amend as follows:

In the claims:

Please cancel claims 2, 3, 8, 9, and 19, and amend claims 1, 4, 5, 7, and 10-14, and add claims 20-21, as follows:

1. (Twice Amended) A method for etching a feature in an integrated circuit wafer incorporating at least one layer of organosilicate glass dielectric, the method comprising:

positioning the wafer in a reaction chamber;

introducing a flow of etchant gas mixture including C4F8, CH2F2, oxygen, and CF4 into the reaction chamber; [and]

striking a plasma with the atchant gas in the reaction chamber; and

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